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09/280385 10/30/01

Paper No. #11

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(19) **United States**(12) **Patent Application Publication**  
**Harari et al.**(10) Pub. No.: **US 2002/0046318 A1**(43) Pub. Date: **Apr. 18, 2002**(54) **FLASH EEPROM SYSTEM****Publication Classification**(76) Inventors: **Ellyahou Harari**, Los Gatos, CA (US);  
**Robert D. Norman**, San Jose, CA  
(US); **Sanjay Mehrotra**, Milpitas, CA  
(US)(51) Int. Cl.<sup>7</sup> ..... **G06F 12/00**  
(52) U.S. Cl. .... **711/103; 711/163; 365/185.3;**  
**365/185.33**Correspondence Address:  
**Michael G. Cleveland**  
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**San Jose, CA 95110 (US)**(57) **ABSTRACT**(21) Appl. No.: **10/000,155**(22) Filed: **Oct. 30, 2001****Related U.S. Application Data**(60) Continuation of application No. 09/280,385, filed on  
Mar. 29, 1999, which is a continuation of application  
No. 08/771,708, filed on Dec. 20, 1996, now pat-  
ented, which is a continuation of application No.  
08/174,768, filed on Dec. 29, 1993, now patented,  
which is a continuation of application No. 07/963,  
838, filed on Oct. 20, 1992, now patented, which is a  
division of application No. 07/337,566, filed on Apr.  
13, 1989, now abandoned.

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

